Parallel Computer Models

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John von Neumann

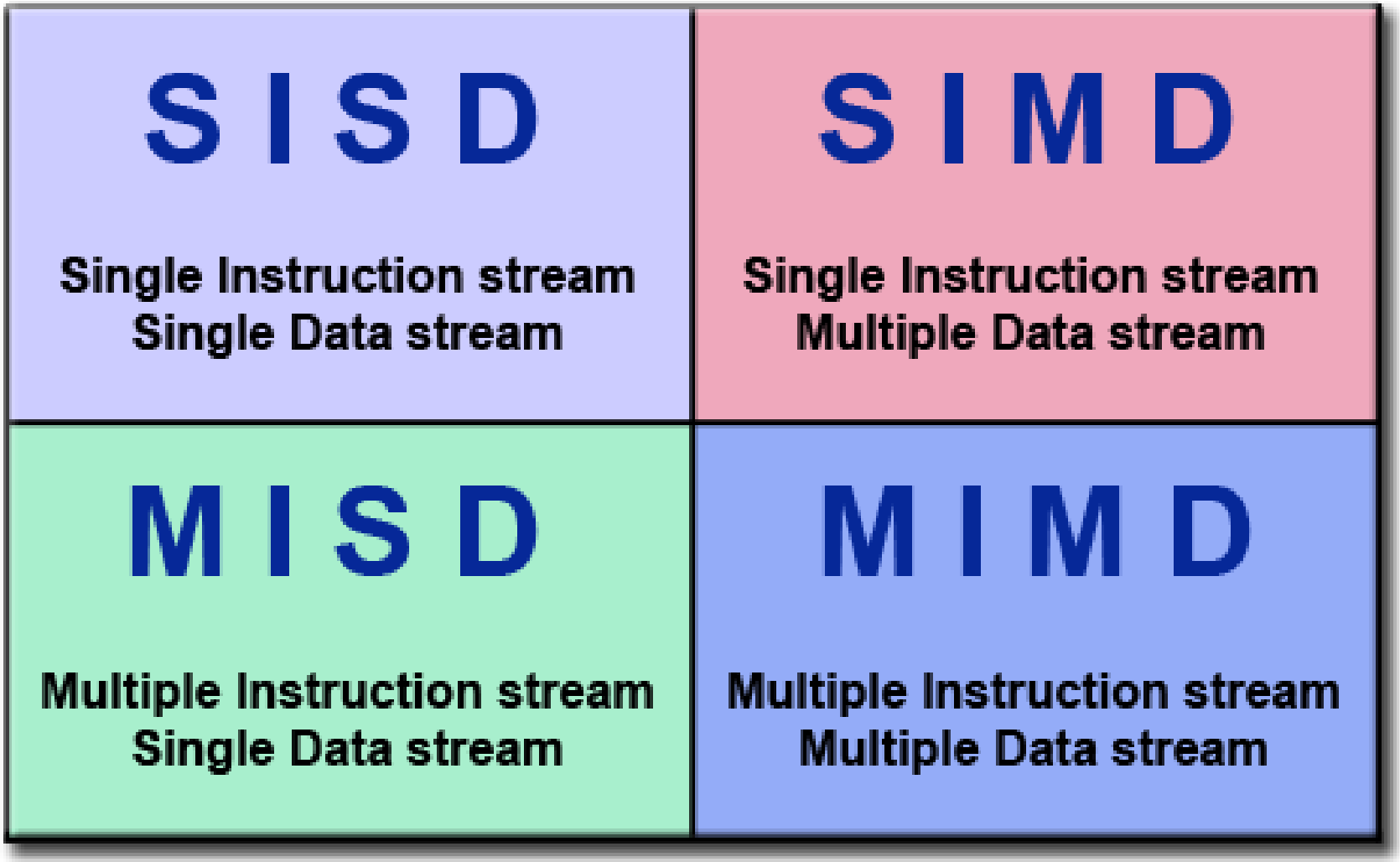
- Stored-program computer
- Read/write, random access memory is used to store both program instructions and data
  - Program instructions are coded data which tell the computer to do something
  - Data is simply information to be used by the program
- Control unit fetches instructions/data from memory, decodes the instructions and then ***sequentially*** coordinates operations to accomplish the programmed task.
- Arithmetic Unit performs basic arithmetic operations
- Input/Output is the interface to the human operator

Flynn's Taxonomy of Parallel Architectures

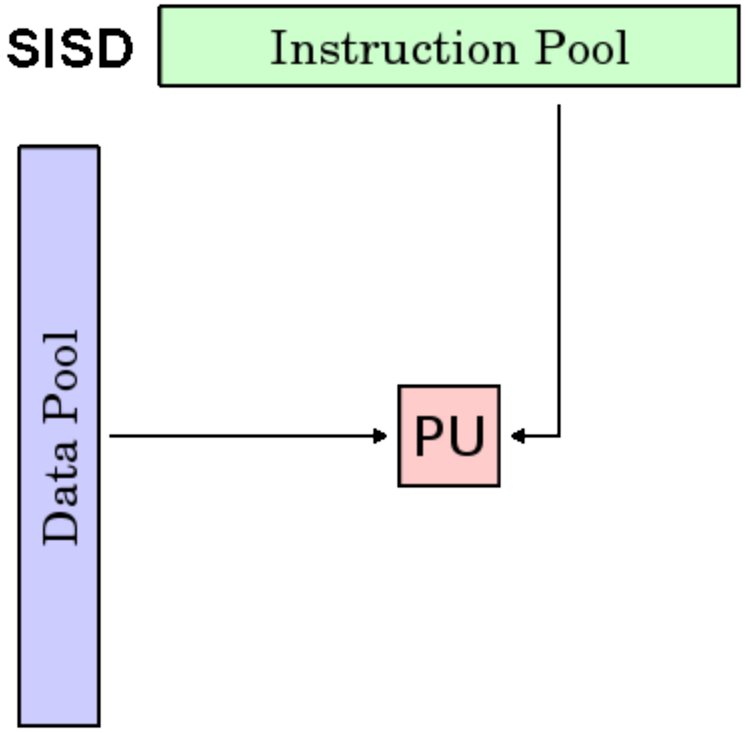
- Flynn's taxonomy distinguishes multi-processor computer architectures according to how they can be classified along the two independent dimensions of ***Instruction Stream*** and ***Data Stream***.
- Each of these dimensions can have only one of two possible states: ***Single*** or ***Multiple***.

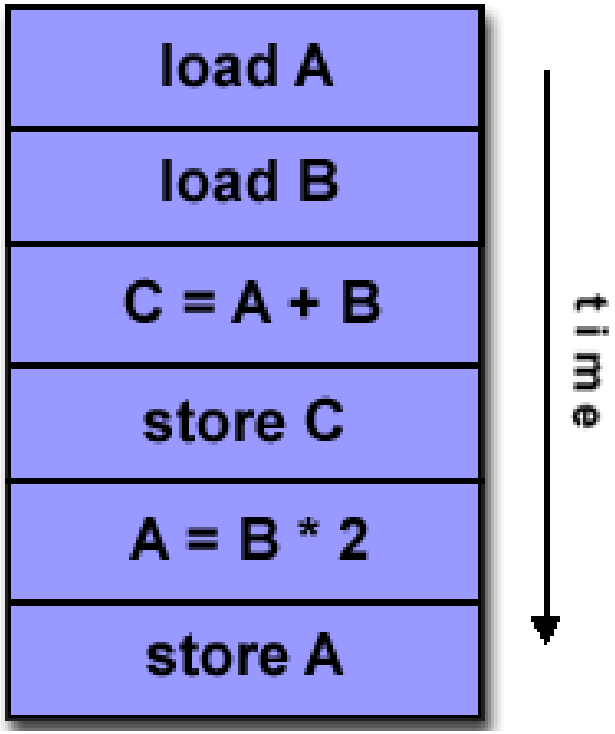
- **Instructions Stream :** sequence of instructions executed by the computer.

- **Data Stream:** sequence of data including input, temporary or partial results referenced by instructions.


S I S D
Single Instruction stream
Single Data stream
S I M D
Single Instruction stream
Multiple Data stream
M I S D
Multiple Instruction stream
Single Data stream
M I M D
Multiple Instruction stream
Multiple Data stream

Single Instruction, Single Data (SISD) / Scalar





UNIVAC1

IBM 360

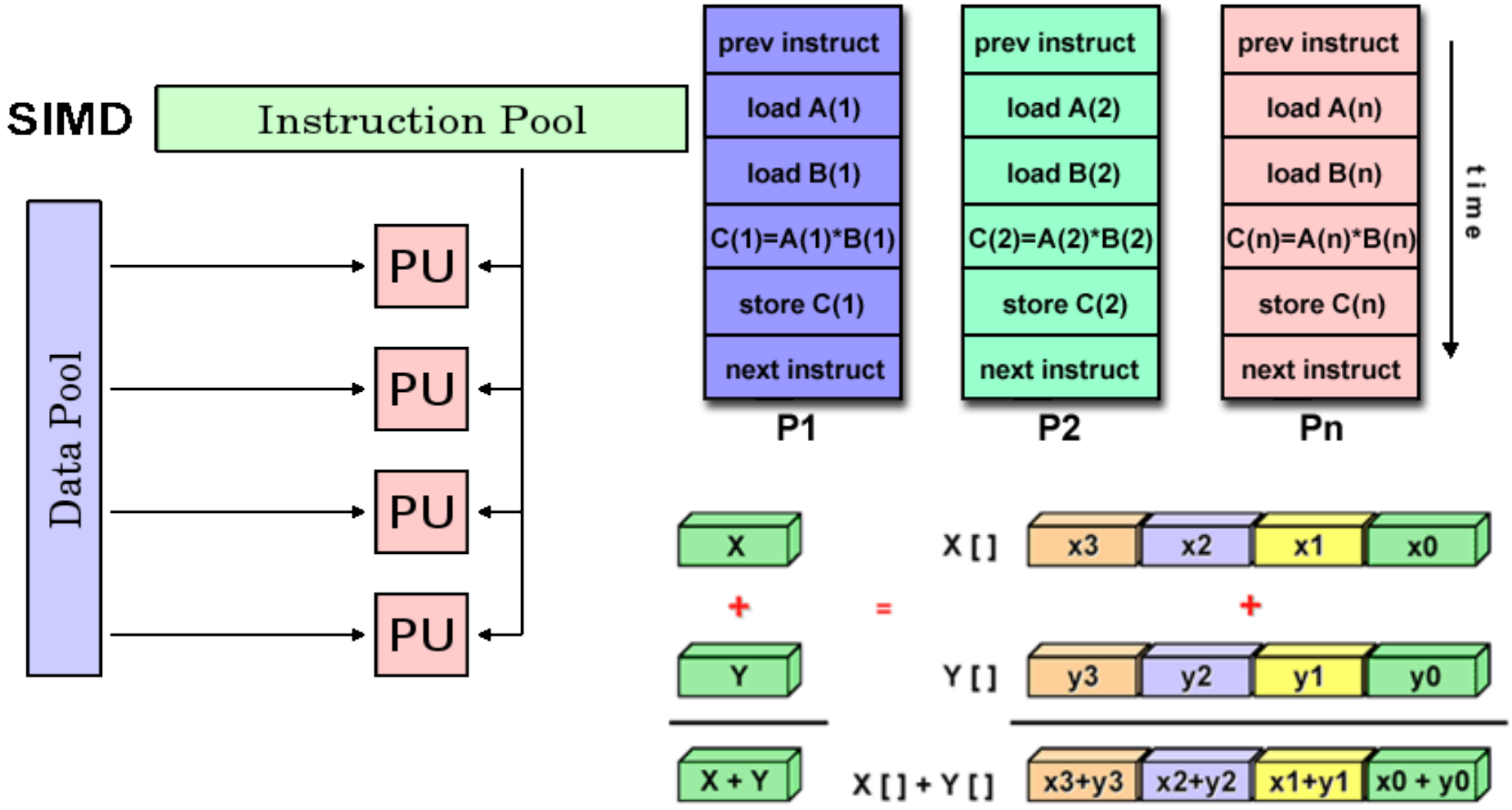
CRAY1

CDC 7600

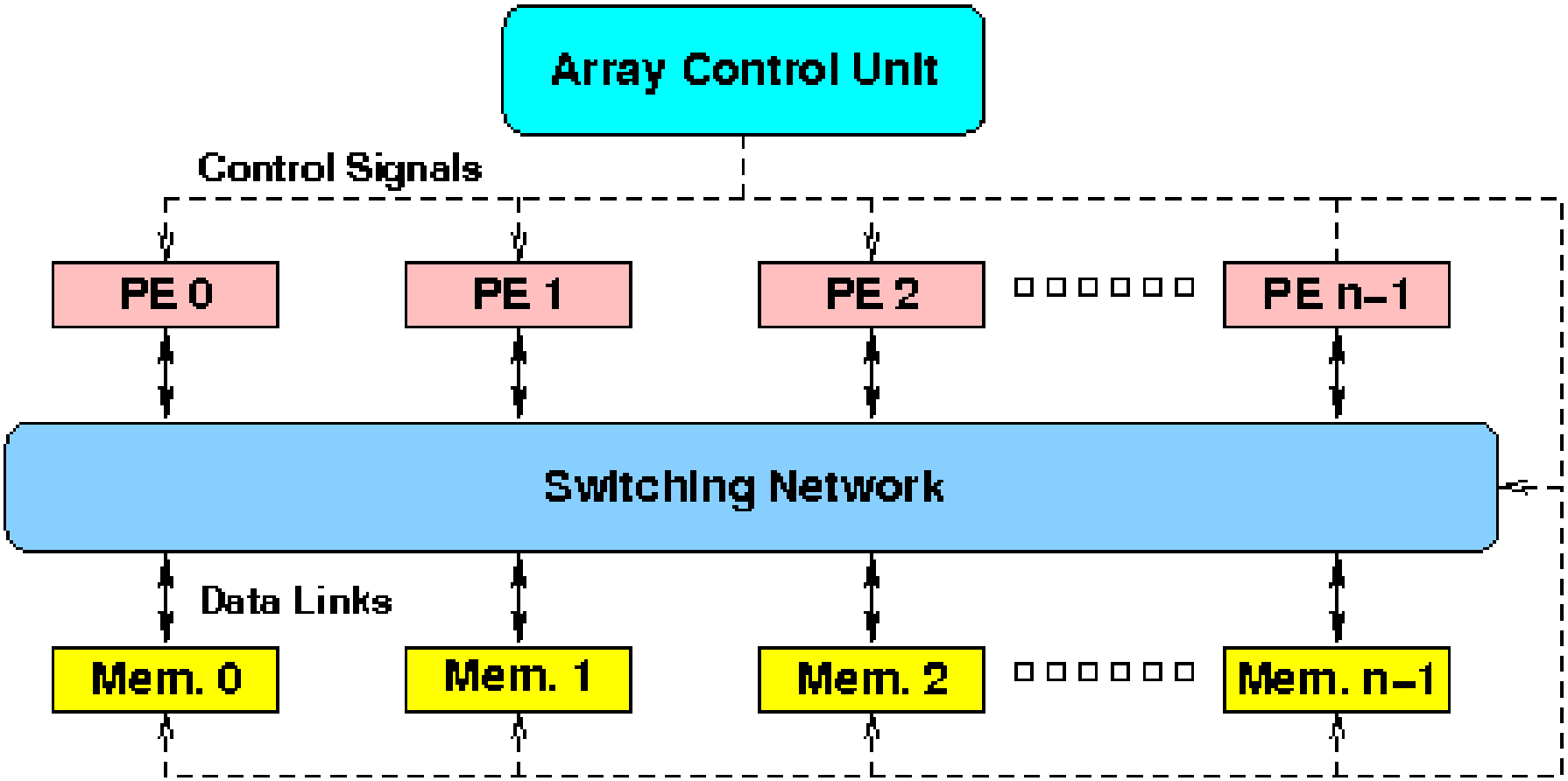
PDP1

Dell Laptop

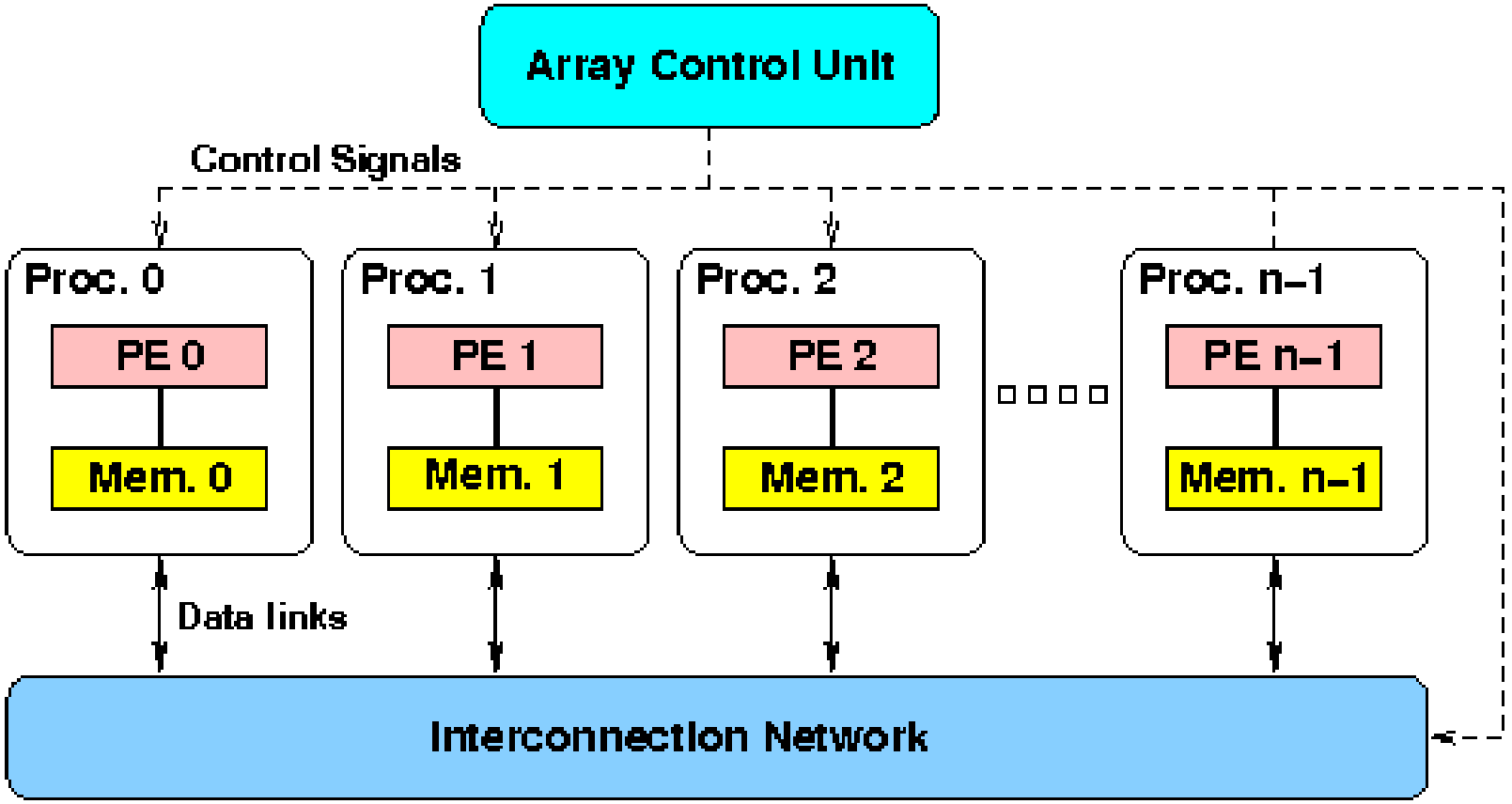
Single Instruction, Multiple Data (SIMD) / Vector



SIMD with shared memory

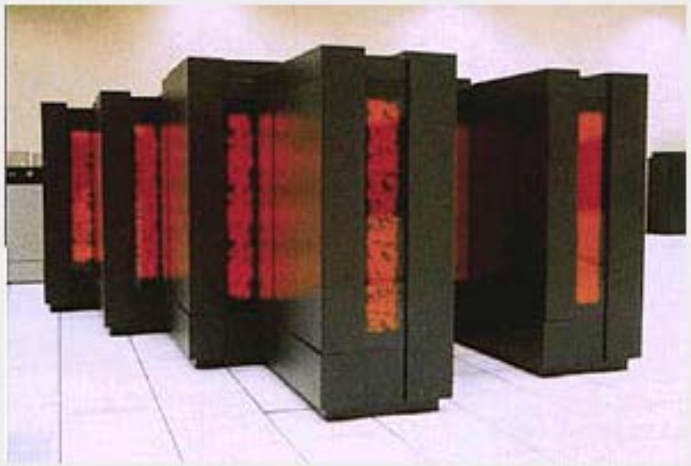


SIMD with Distributed memory

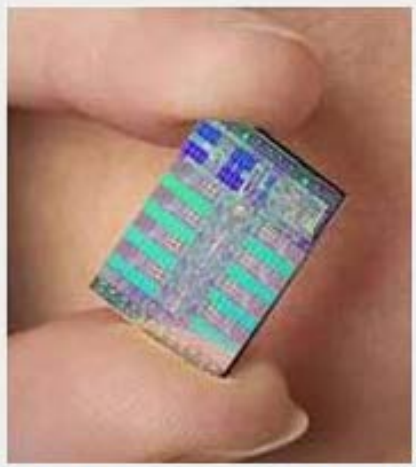


Cray X-MP

Cray Y-MP

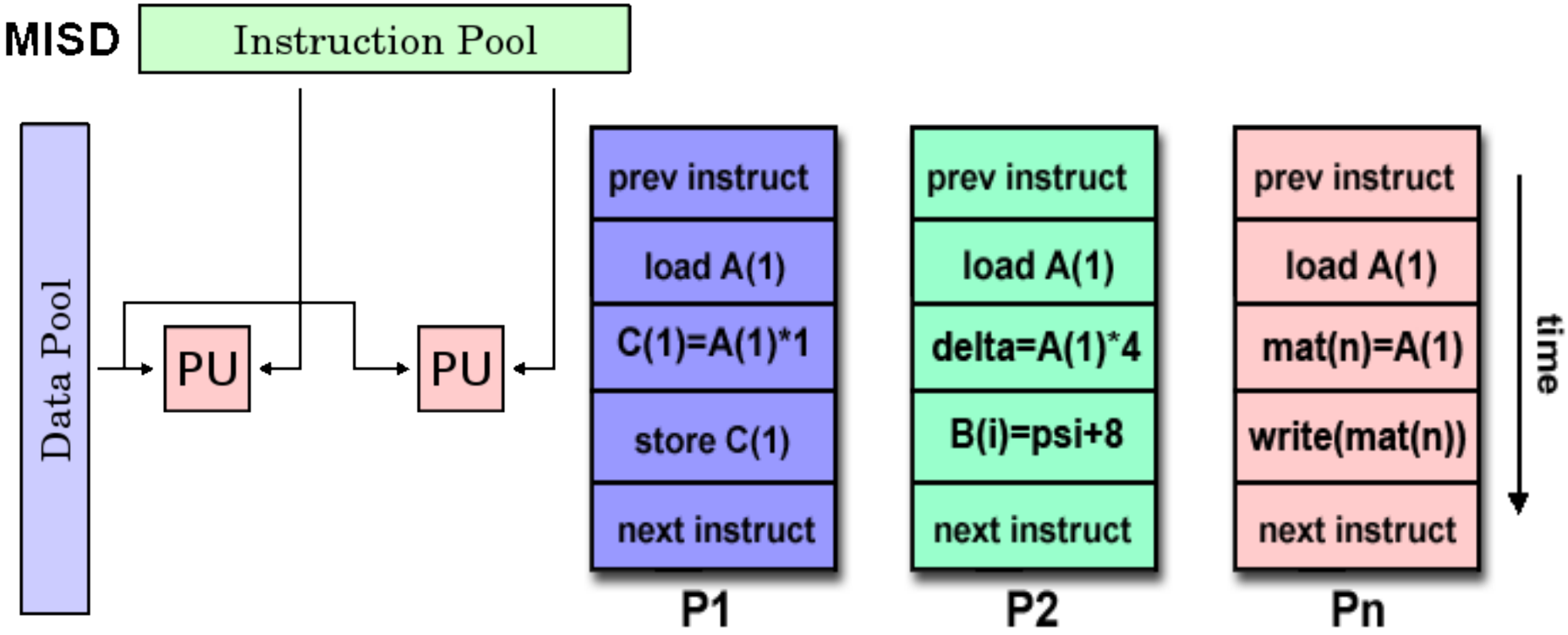


Thinking Machines CM-2

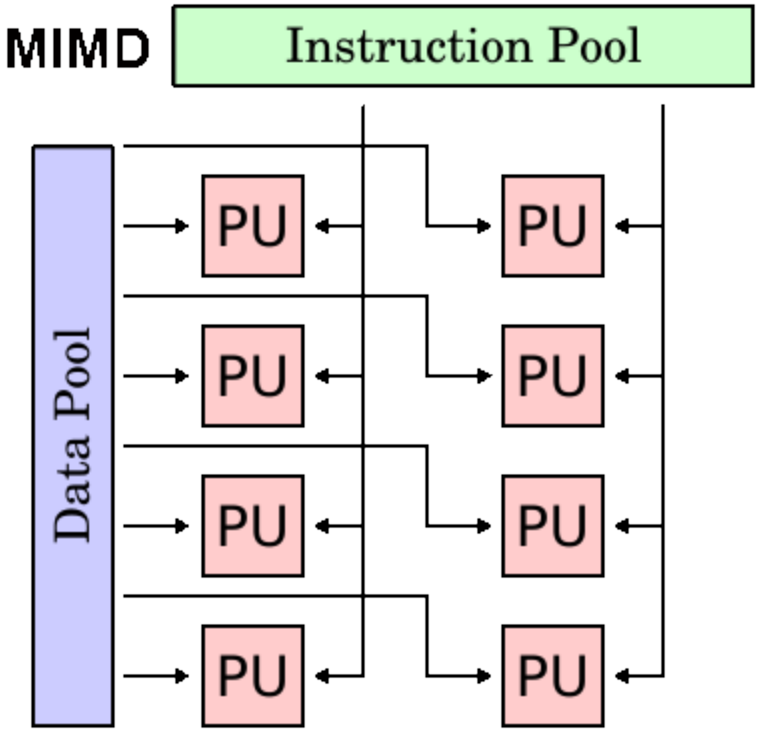


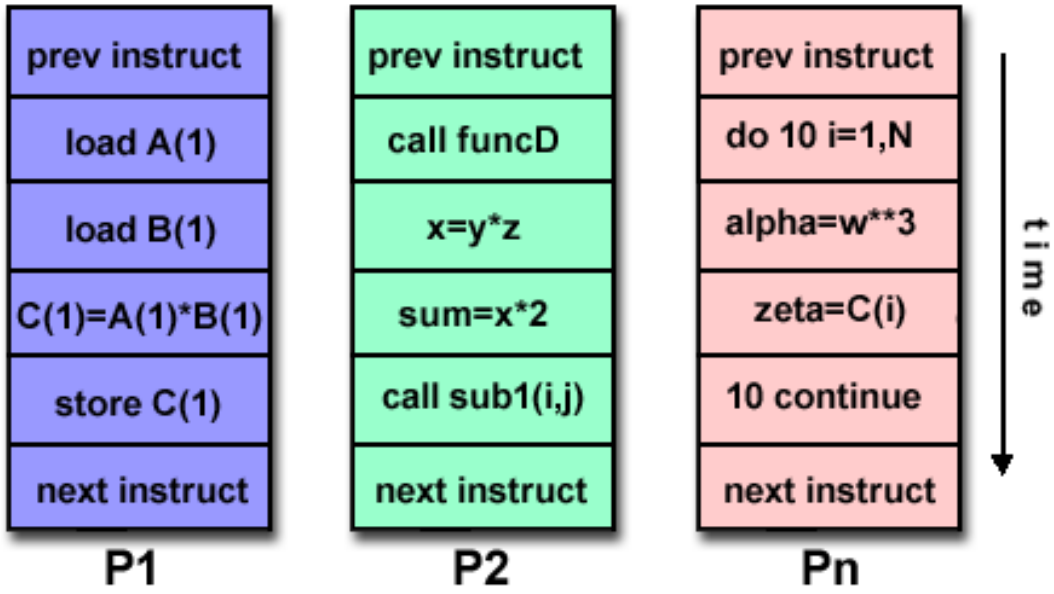
Cell Processor (GPU)

Multiple Instruction, Single Data (MISD) / Systolic

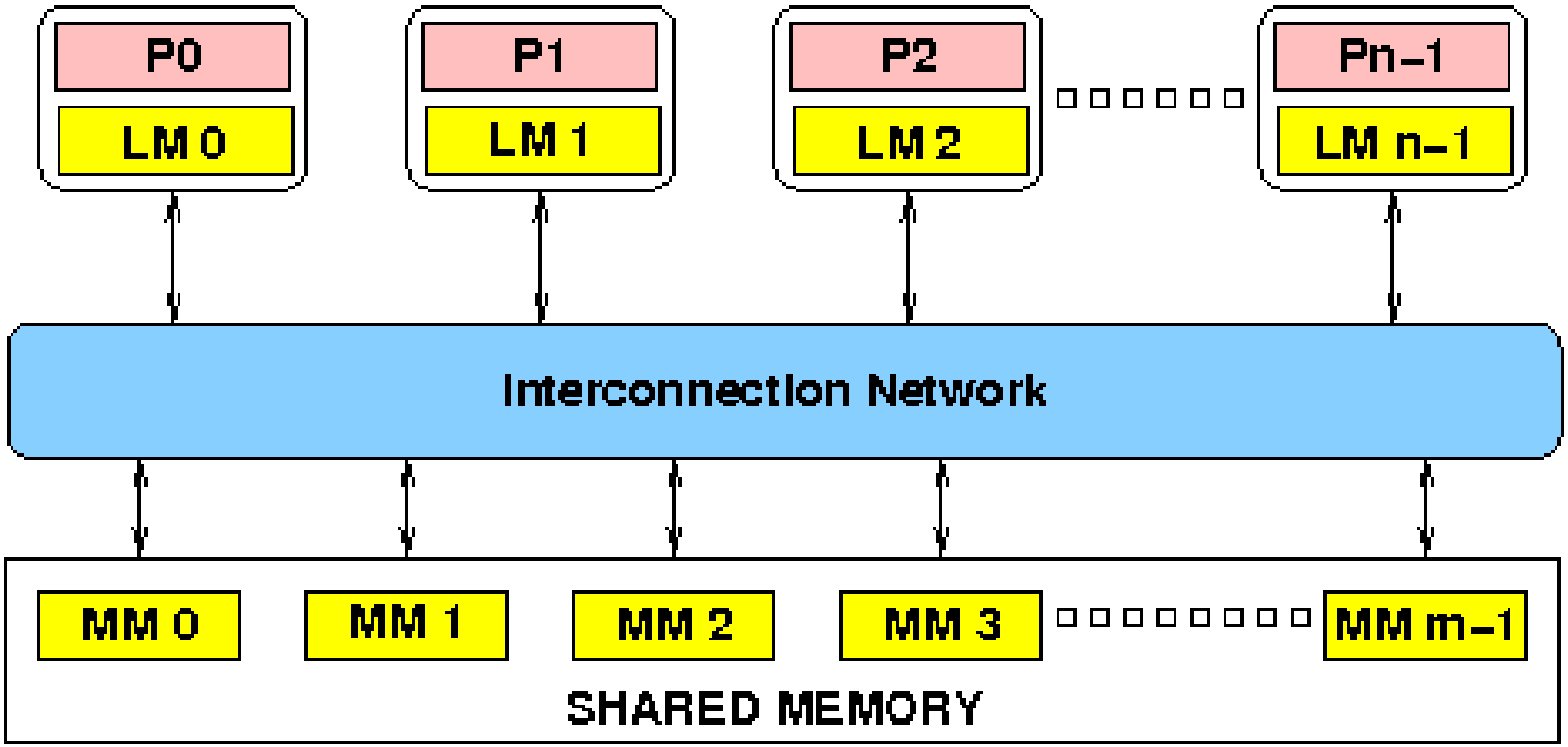


Multiple Instruction, Multiple Data (MIMD) / Parallel





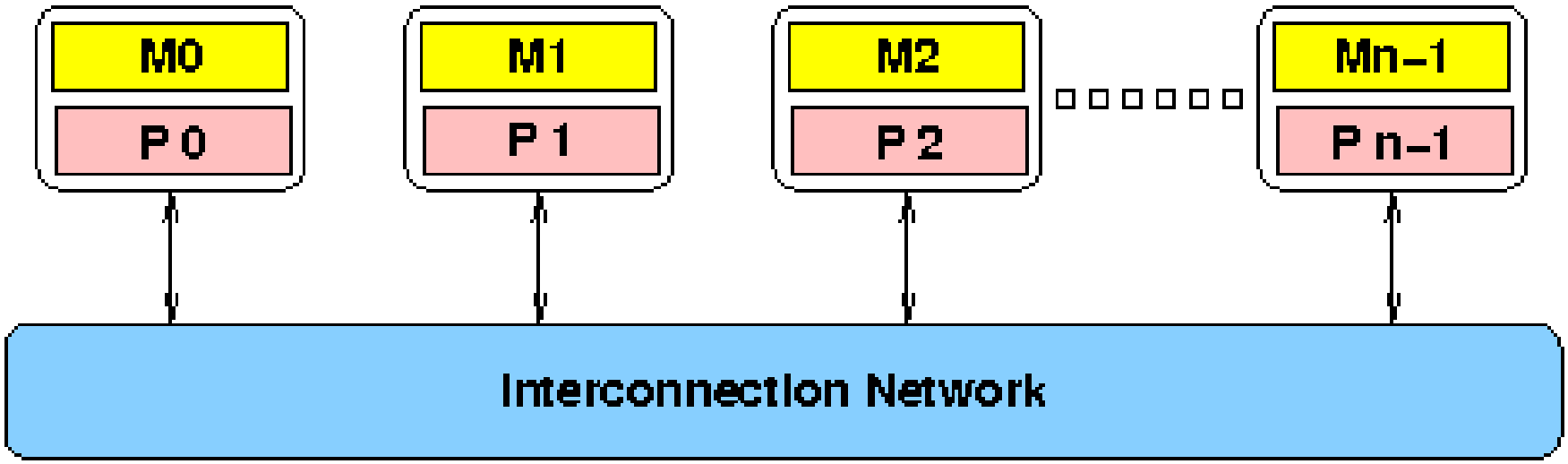
MIMD Shared Memory



Shared Memory Organization

- Inter-processor coordination is accomplished by reading and writing in a global memory shared by processors.
- Typically consists of servers that communicate through a bus and cache memory controller.

MIMD with Distributed Memory / Message Passing



Message Passing Organization

- Each processor has access to its own local memory.
- Communications are performed via send and receive operations.
- Message passing multiprocessors employ static networks in local communications

IBM POWER5

HP/Compaq Alphaserver

Intel IA32

AMD Opteron

Cray XT3

IBM BG/L

Parallel Processing

- Parallel processing uses multiple pieces of HARDWARE, (i.e.processors), to simultaneously process the same task (i.e instructions + data elements).
- These processors can be multiples on single computer or on a number of computers connected by a network, or combination of both.
- Since the load of work,is spread over multiple processors or machines and running all in sync at the same time the overall through-put is multiplied and the output is received in a much short amount of time.
- The different processors access the data elements through shared memory.
- The largest computers using parallel processing architecture, known as Super-Computers, have hundreds of thousands of processors.

Vector Processing

- In Vector processing, a specially designed instruction set (i.e. piece of software), contains operations that can perform processing on MORE THAN ONE data element at the same time.
- Vector processing architecture is non-scalar. Scalar, which is used in the vast majority of computers today, processes just ONE data element at time using multiple instructions.
- Vector computers are equipped with scalar and vector hardware or appear as SIMD machines.

Thank You !!!!